8. The device structure of claim 1 further comprising:

a plurality of trench isolation regions in a semiconductor substrate that surround a device region,

wherein the intrinsic base includes a polycrystalline region over the trench isolation regions, the polycrystalline region comprised of polycrystalline semiconductor material and including first sections and second sections having different thicknesses.

9. The device structure of claim 8 wherein the extrinsic base includes a polycrystalline region that combines with the polycrystalline region of the intrinsic base to fill open spaces between the first sections to reduce the different thicknesses.

10. The device structure of claim 9 wherein the extrinsic base is comprised of Si_xGe_{1-x}.

11. The device structure of claim 1 further comprising:

an insulating layer on the silicide layer.

12. The device structure of claim 11 wherein the insulating layer has a top surface, and the first spacers project above the top surface of the insulating layer.

13. A hardware description language (HDL) design structure encoded on a machine-readable data storage medium, the HDL design structure comprising elements that when processed in a computer-aided design system generates a machine-executable representation of a bipolar junction transistor, the HDL design structure comprising:

an intrinsic base including a top surface;

an extrinsic base on the top surface of the intrinsic base;

a silicide layer on the extrinsic base;

a plurality of first spacers having an outer surface, the first spacers oriented to project vertically relative to the top surface of the intrinsic base, the first spacers arranged to line an emitter window therebetween, and the emitter window extending through extrinsic base and the silicide layer to the top surface of the intrinsic base; and

an emitter including a portion disposed in the emitter window and a head protruding out of the emitter window, the portion of the emitter in contact with the intrinsic base, and the portion of the emitter having a plurality of sidewalls that border the first spacers and that are separated from the extrinsic base and the silicide layer by the first spacers,

wherein the silicide layer and the extrinsic base each terminate at the outer surface of the first spacers so that the silicide layer and the extrinsic base are aligned relative to each other and relative to the portion of the emitter by the first spacers.

14. The HDL design structure of claim 13 wherein the HDL design structure comprises a netlist.

15. The HDL design structure of claim 13 wherein the DHL design structure resides on storage medium as a data format used for the exchange of layout data of integrated circuits.

16. The HDL design structure of claim 13 wherein the HDL design structure resides in a programmable gate array.

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